

REMARKS

Claims 2-16 and 18-25 were pending when last examined. All pending claims are shown in the detailed listing above.

Claim Rejections – 35 USC § 112

Claims 18-20 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. According to the Examiner, “Regarding claim 18, the recitation ‘at most three transistors operable to provide signal currents’ on line 4 is indefinite because it is misdescriptive. Figure 1 of the present application shows that there are more than 3 transistors (12, 14, 16, 18, 20, 22) in the circuit that provide signal currents.” Applicants respectfully traverse.

Claim 18 is not indefinite. The recitation of “at most three transistors operable to provide signal currents” in claim 18 is fully supported and described in the specification. For example, referring to FIG. 1, the specification recites:

In precision buffer circuit 10, in some embodiments, only transistors 16, 18, and 24 are conducting signal currents. The remaining transistors—i.e., transistors 12, 14, 18, 20, and 22—are conducting only bias currents, thus operating to provide relatively constant current. As such, precision buffer circuit 10 may provide faster operation within a given operational range of $\Delta V/\Delta t$ for the input signal V_{in} compared to previously designed buffer circuits which have more transistors or components providing signal currents.

Application, page 5, second full paragraph. As such, the language of claim 18 particularly points out and distinctly claim subject matter which Applicants regard as the invention, in one embodiment. Thus, the rejection under 35 U.S.C. § 112, second paragraph should be withdrawn.

Claim Rejections – 35 USC § 102

Claims 18-20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Xu (US 6,066,985). Applicants respectfully traverse.

Claim 18 recites, *inter alia*, “A buffer circuit comprising... at most three transistors operable to provide signal currents.” Nowhere in Xu is such limitation disclosed or taught. As such, Xu does not anticipate claim 18.

For at least the reasons discussed above, Applicants respectfully request that the rejection of claim 18 under 35 U.S.C. § 102(b) be withdrawn and this claim be allowed. Furthermore, because claims 19 and 20 depend from claim 18 and include further limitations, the Applicants respectfully request that the rejection of these dependent claims under 35 U.S.C. § 102(b) also be withdrawn and that claims 19 and 20 be allowed.

Allowable Subject Matter

Applicants appreciate the Examiner’s allowance of Claims 2-16 and 21-25, but respectfully comment on the Examiner’s reasons for allowance. Applicants note that the Examiner has slightly misquoted the language from the claims. In particular, the Examiner states, “Claims 2-16 and 21-25 are allowed because the prior art of records (US 6,066,985) fails to teach or suggest a buffer circuit comprising a third transistor having the source coupled to the source of the second transistor and the gate coupled to the drain of first transistor as called for in claims 2, 7, 9, 10 and 21.” Each of claims 2, 7, 9, 10, and 21 actually recite, in pertinent part, “A buffer circuit comprising...a third transistor having a gate, a source, and a drain, wherein the gate of the third transistor is connected to the drain of the first transistor, wherein the source of the third transistor is connected to the output terminal and to the source of the second transistor.”

CONCLUSION

Applicants respectfully request that the pending claims be allowed and the case passed to issue. Should the Examiner wish to discuss the Application, it is requested that the Examiner contact the undersigned at (415) 772-7428.

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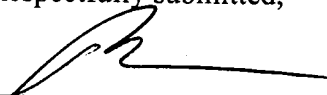
9/22/06

Date

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